ARGUMENTS/REMARKS

Favorable reconsideration of this application, as amended, is respectfully requested.

To reduce the issues and expedite the allowance of this application, and without acceding to the rejections, Claims 1-5, 14-17, 28-30, and 36-38 have been cancelled. The subject matter of Claims 14 and 15 has been incorporated in amended Claim 6. The subject matter of Claims 28 and 29 has been incorporated in amended Claim 20. Claim 20 has also been amended to recite that the conductive type of the first semiconductor region is a p type and that of the third semiconductor region is an n type, and that a second voltage is applied to the first semiconductor region `in the first period and thereby the third semiconductor region is charged through the first semiconductor region up to the second voltage. Amended Claim 31 also recites that the conductive type of the first semiconductor region is a p type and that of the third semiconductor region is an type, and that a second voltage is applied to a first semiconductor region in a first period and thereby the third semiconductor region is charged through the first semiconductor region up to the second voltage.

The inventions recited in amended Claims 6 and 20 have effects of applying continuously the third voltage to the third semiconductor region during the first to third periods. The inventions recited in amended Claims 20 and 31 have effects of charging the third semiconductor region through the first semiconductor region up to the second voltage during the first period, and have effects of maintaining the third semiconductor region in a floating state during the first to third periods. Since the third semiconductor region is maintained at the third voltage (second voltage) even during the second period of determining the threshold voltage of the memory cell, maintaining the third semiconductor region at such voltage is achieved by simply increasing the first semiconductor region up to the second voltage during the third period of pulling out electrons into the first semiconductor region again, thereby allowing shortening of a period of time required until the first semiconductor region reaches the second voltage and allowing shortening of a period for deletion. See, e.g., without limitation, page 29, lines 20-26; and page 34, lines 5-24 of the specification.

Claims 1-38 were rejected under 35 U.S.C. § 102(b) as being anticipated by Akaogi et al. (U.S. Patent No.

5,761,127). This rejection is respectfully traversed with regard to the claims now presented.

Akaogi et al. disclose the inner p-type well 138 as a component similar to the first semiconductor region in the present invention, and the outer n-type well 136 as a component similar to the third semiconductor region, respectively (Fig. 35, Column 24, lines 4-10). Fig. 35 shown in Akaogi et al. indicates that "V_L = +10 V" (a typographical error of -10 V) is applied to the control gate electrode 124a; "+10 V" is applied to the inner p-type well 138; and "V_L = +10 V" is applied to the outer n-type wll 136. However, since Fig. 35 is a modification of Fig. 34, Akaogi et al. only teach an example of the voltage applied at the time of pulling out electrons into the inner p-type well 138. That is, Akaogi et al. only disclose an example of the voltage applied during the first period described in the present invention.

As discussed above, one of the aspects of the present invention has effects of continuously maintaining the third semiconductor region at a predetermined voltage (the second voltage or third voltage) during the first period of pulling out electrons, the second period of determining the threshold voltage, and the third period of pulling out

electrons again. In contrast, Akaogi et al. do not even disclose determining the threshold voltage after pulling out electrons and do not teach or suggest how to control the voltage of the outer n-type well 136 in determining the threshold.

Accordingly, Claims 6, 20, and 31, as well as the claims dependent upon Claims 6 and 20, distinguish patentably from Akaogi et al. and should be allowed.

The invention recited in Claim 32 has an effect of separating the third semiconductor region at intervals of units of the predetermined number of memory cells in a plurality of memory cell groups, thereby allowing reduction of parasitic capacitance adhering to one of the third semiconductor region and allowing shortening of a period of time for deletion. See, e.g., without limitation, page 40, lines 24 to page 41, line 3; page 41, lines 17-20; and page 44, line 26 to page 45 line 5.

In contrast, Akaogi et al. disclose the outer n-type well 136 (see Fig. 35) as a component similar to the third semiconductor region in the present invention. However, as is apparent from Fig. 35, the outer n-type well 136 is not divided, unlike the present invention. In addition, Akaogi et al. do not teach or suggest dividing the outer n-type

well 136 anywhere. Accordingly, Claim 32 and the claims dependent thereon distinguish patentably from Akaogi et al. and should be allowed.

The rejection based on Akaogi et al. refers in very general terms to certain portions of the Akaogi et al. disclosure, asserts that certain claims contain limitations similar to those discussed in Claims 6-15 and that the apparatus discussed in Claims 6-15, etc. would perform the method as claimed. Applicants respectfully traverse these assertions.

Moreover, in view of the foregoing remarks, if any of the claims now presented is rejected again based on Akaogi et al., Applicants respectfully request that each of the elements recited in the claims and alleged to be found in Akaogi et al. be specifically identified in the reference.

Accordingly, this application is now believed to be in condition for allowance.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this

paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

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